Claims

[c1] An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), each said NFET and said PFET having a channel region disposed in a single-crystal layer of a first semiconductor, wherein a stress is applied at a first magnitude to a channel region of said PFET but not to a channel region of said NFET by a layer of a second semiconductor which is lattice-mismatched to said first semiconductor, said layer of second semiconductor being formed in source and drain regions of said PFET a first distance from said channel region of said PFET, and said layer of said second semiconductor further being formed in source and drain regions of said NFET at a second distance from said channel region of said NFET, said second distance being greater than said first distance.

[c2] The integrated circuit of claim 1 wherein said first semiconductor and said second semiconductor are silicon containing semiconductor materials having a composition according to the formula Si_xGe_y, wherein x and y are

percentages, said first semiconductor ranging in composition between xyto xyand said second semiconductor ranging in composition between xyto xywherein y for said second semiconductor is always greater than y for said first semiconductor.

[c3] The integrated circuit of claim 1 wherein said single-crystal region of said first semiconductor has a main surface defined by a level of a gate dielectric formed on said channel regions of said NFET and said PFET and said layer of said second semiconductor is formed above said main surface.

[c4] The integrated circuit of claim 3 further comprising a layer of silicide formed over said layer of said second semiconductor.

[c5] The integrated circuit of claim 1 wherein said first semiconductor consists essentially of a semiconductor selected from the group consisting of silicon, silicon germanium and silicon carbide and said second semiconductor consists essentially of another semiconductor different from said first semiconductor, said another semiconductor selected from the group consisting of silicon, silicon germanium and silicon carbide.

[c6] The integrated circuit of claim 1 wherein said first semi-

conductor consists essentially of silicon and said second semiconductor consists essentially of silicon germanium.

[c7] The integrated circuit of claim 1 wherein said first semiconductor consists essentially of silicon germanium according to a first formula $Si_{x1}Ge_{y1}$, where x1 and y1 are percentages, x1 + y1 = 100%, y1 being at least one percent and said second semiconductor consists essentially of silicon germanium according to a second formula $Si_{x2}Ge_{y2}$, where x2 and y2 are percentages, x2 + y2 = 100%, y2 being at least one percent, wherein x1 is not equal to x2 and y1 is not equal to y2.

[c8] The integrated circuit of claim 1 wherein said first stress is a compressive stress.

[c9] The integrated circuit of claim 6 wherein said second semiconductor consists essentially of silicon germanium having a germanium content of at least one percent.

[c10] The integrated circuit of claim 4 wherein each of said PFET and said NFET further comprise a layer of silicide contacting gate conductors, source regions and drain regions of said PFET and said NFET.

[c11] An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect

transistor (NFET), each said NFET and said PFET having a channel region disposed in a single-crystal layer of a first semiconductor, wherein a first stress is applied to a channel region of said PFET but not to a channel region of said NFET by a layer of a second semiconductor lattice-mismatched to said first semiconductor being formed in raised source and drain regions of said PFET, said layer of said second semiconductor not being formed in raised source and drain regions of said NFET.

[c12] An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET) each having channel regions disposed in single-crystal silicon regions of a substrate wherein a first stress is applied to the channel region of the PFET but not to the channel region of the NFET via a raised lattice-mismatched semiconductor layer consisting essentially of silicon germanium disposed in source and drain regions of the PFET a first distance from said channel region of said PFET and disposed in source and drain regions of the NFET a second distance from said channel region of said NFET, said silicon germanium having a composition according to the formula $Si_x Ge_y$ where x and y are percentages each being at least one percent, x plus y equaling 100 percent.

[c13] A method of fabricating an integrated circuit including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), said NFET and said PFET each having a channel region disposed in a single-crystal region of a first semiconductor, a stress being applied to said channel region of said PFET in a first magnitude and not being applied to said channel region of said NFET at said first magnitude, said method comprising:
forming a PFET gate stack and an NFET gate stack over a single-crystal region of a first semiconductor, said PFET gate stack and said NFET gate stack each having a gate conductor overlying a gate dielectric formed on a main surface of said single-crystal region and first spacers including a first material formed on sidewalls of said gate conductor;
forming second spacers on sidewalls of said first spacers of said PFET gate stack and said NFET gate stack, said second spacers including a second material;
removing portions of said second material from said second spacers of said PFET gate stack selective to said first material while protecting said second material from being removed from said second spacers of said NFET gate stack;
thereafter growing a layer of a second semiconductor on exposed areas of said single-crystal region of said first

semiconductor, said second semiconductor being lattice-mismatched to said first semiconductor, such that a stress is applied to said channel region of said PFET at a first magnitude and not applied to said channel region of said NFET at said first magnitude; and
fabricating source and drain regions of said PFET and fabricating source and drain regions of said NFET.

[c14] A method as claimed in claim 13 wherein said PFET further comprises raised source and drain regions formed above a level of said main surface in said layer of said second semiconductor.

[c15] A method as claimed in claim 14 wherein said NFET further comprises raised source and drain regions formed above a level of said main surface in said layer of said second semiconductor.

[c16] A method as claimed in claim 14 wherein said source and drain regions of said NFET are formed in said layer of said first semiconductor.

[c17] A method as claimed in claim 15 wherein said raised source and drain regions of said NFET are spaced by said first and second spacers from said NFET gate stack.

[c18] The method of claim 17 further comprising forming a self-aligned silicide (salicide) in said raised source and

drain regions of said PFET and said NFET.

[c19] The method of claim 18 further comprising forming a self-aligned silicide (salicide) over polysilicon portions of said gate conductors of said PFET and said NFET.

[c20] The method of claim 19 wherein said silicide includes a silicide of cobalt.

[c21] The method of claim 13 wherein said first semiconductor comprises silicon and said second semiconductor comprises silicon germanium, said silicon germanium having a germanium content of at least one percent.

[c22] The method of claim 21 wherein said lattice-mismatched second semiconductor applies a compressive stress.

[c23] The method of claim 13 further comprising halo implanting areas of said single-crystal region masked by gate conductors of said PFET gate stack and said NFET gate stack prior to forming said first spacers.

[c24] The method of claim 13 further comprising extension implanting areas of said single-crystal region masked by gate conductors of said PFET gate stack and said NFET gate stack prior to forming said first spacers.

[c25] The method of claim 19 further comprising forming third spacers on sidewalls of said second spacers prior to re-

moving portions of said second material from said second spacers, the sidewalls of said third spacers defining spacings between said source and drain regions and said channel region of said PFET.

[c26] The method of claim 25 further comprising protecting said first and second spacers formed on said NFET gate stack by a patterned block mask when removing said portions of said second spacers from said PFET gate stack.

[c27] The method of claim 13 further comprising forming a coating on an NFET active area of said single-crystal region of first semiconductor to prevent said second semiconductor layer from being grown on said NFET active area.

[c28] The method of claim 13 wherein said layer of said second semiconductor is grown selectively.